Comparative Analysis of Three Phase 2-Level VSI with 3-Level and 5-Level DCMLI Using CB-SVM

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***Abstract*— Analysis of Diode-Clamped Multilevel inverter using IGBT's has been proposed in this paper. The pulses for the inverters have been developed by using Carrier based Space Vector Modulation Technique (CB-SVM). Design and simulation of two-level, three-level and five-level inverter in Matlab software using Carrier based space vector modulation technique is presented. Comparison of the performance in terms of output voltage and total harmonics distortion and the results of simulation are presented.**

Keywords*— *Two-level inverter, three level inverter, five level inverter, Diode Clamped Multilevel Inverter(DCMLI) , Carrier based Space Vector Modulation (CBSVM), Voltage Source Inverter(VSI).

I. INTRODUCTION

In power conversion technology, multilevel is a good technology in the area of power electronics. The most attractive applications of this technology are in the medium-to high-voltage range i.e. 2-13 kV, and include motor drives, power distribution, power quality and power conditioning applications. In multilevel power converters, the high output voltage is synthesized from many discrete smaller voltage levels. The selection of the best multilevel topology and the best control strategy is often not clear for each given application. In the study of DC/AC multilevel power conversion technologies, it do not require power regeneration, several attractive topological, modulation and power semiconductor device choices present themselves [1]-[4].The Two-Level inverter topology has attracted attention in low power, low voltage drive applications. Whereas Three-Level inverter topology has attracted attention in high power high performances voltage drive applications. The Main purpose of these two-level and three-level inverter topologies is to provide a three phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. The two-level inverter is composed of only one switching cell per phase but the three-level inverter has two switching cell per phase. Three level diode clamped (Neutral point) inverter is most favourable among the various multi level configuration. Using enough levels the multi-level inverter generates approximately a sinusoidal voltage waveform with very low harmonic distortion [2]-[6].

The multilevel inverter has been used renewable energy generation and distribution also in power conditioning devices. The different multilevel inverter structures such as cascaded H-bridge, diode clamped and flying capacitor multilevel inverter are available [7].In this paper the analysis of two, three and five-level diode clamped multilevel inverter has been simulated using IGBT's. Pulses for the switches have been obtained using CB-SVM technique and the output voltage, current and THD analysis of these inverters are studied.

II. DIODE CLAMPED MULTILEVEL INVERTER

A. Two Level Diode Clamped Inverter

The three phase two level voltage source diode clamped inverter is shown in the Fig.1. The inverter is composed of six groups of active switches, Q1 to Q6, with a free-wheeling diode in parallel with each switch.Each switch group consists of two or more IGBT's or GCT switching devices connected in series for dc operating voltage of the inverter This paper focuses on CB-SVM for the high power two-level inverter, where the device switching frequency is normally below 1 kHz. The conventional SVM scheme usually generates both even- and odd-order harmonics voltages. The mechanism of even-order harmonic generation is analyzed, and a modified Carrier based Space Vector Modulation Technique (CB-SVM). Scheme is presented for even-order harmonic elimination.

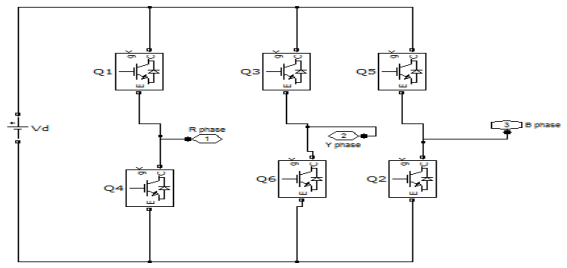

Fig.1. Three phase two-level diode clamped inverter

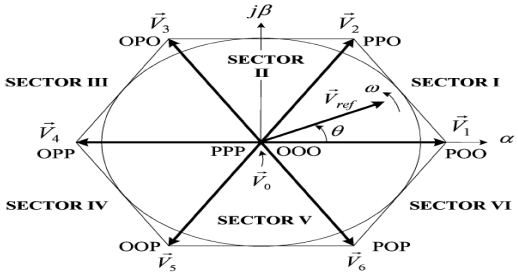

Fig. 2. Space Vector diagram for two-level inverter

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B. *Three Level Diode Clamped Inverter*

Circuit diagram of a three-level inverter is as shown in fig 3 and the switching states of each phase of the inverter are listed in Table I. There are three kinds of switching states P, O, and N in each phase, so there exist 27 switching states in three phase three level inverter. The basic principle of the proposed SVPWM method can be explained by using the space–vector diagram of a three-level inverter**.** The space–vector diagram of a three-level inverter, shown in Fig.4. So, if these six small hexagons are shifted toward the centre of the inner hexagon by Vdc/3, the space–vector diagram of a three-level inverter is simplified to that of a two-level inverter. The following two steps have to be taken for simplify into the space–vector diagram of a two-level inverter First, from the location of a given reference voltage, one hexagon has to be selected among the six hexagons. Secondly the original reference voltage vector has to be subtracted by the amount of the centre voltage vector of the selected hexagon. By these two steps, the three-level space–vector plane is transformed to the two-level space–vector plane.

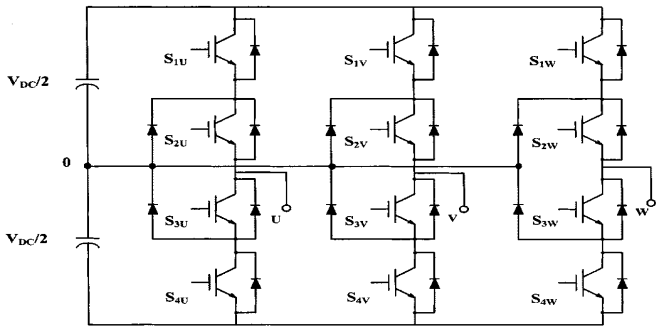

Fig. 3. Three Phase three-level diode-clamped inverter

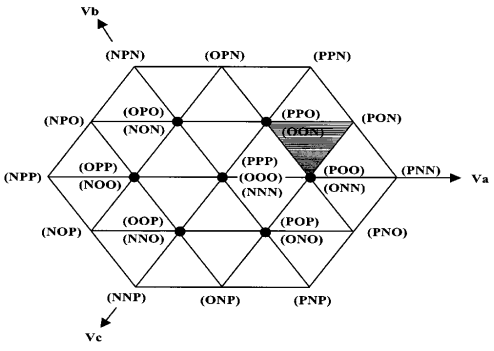

Fig.4. Space vector diagram of three level inverter

TABLE I. SWITCHING STATE AND TERMINAL VOLTAGE OF THREE LEVEL INVERTER

Switching Indication	Switching Sequence				Voltage
	S_1	S_2	S_3	S_4	
P	1	1	0	0	Vdc/2
O	0	1	1	0	0
N	0	0	1	1	-Vdc/2

C. *Five Level Diode Clamped Inverter*

Circuit diagram of a five-level inverter is as shown in fig 5.The space vector diagram of a five level inverter can be thought that is composed of six small hexagons that are the space vector diagrams of the three level inverters as shown in fig.6. Two steps have to be taken for simplify into the space vector diagram of a three level inverter Firstly. From the location of a given reference voltage, one hexagon has to be selected among the six hexagons. We put the center voltage of the selected hexagon from the original reference voltage Secondly. By these two steps, the five level space vector planes is transformed to the three level space vector plane. The space vector diagram of the three level inverter can be combination of six small hexagons of space vector diagram of conventional two level inverter**.**To simplify into the space vector diagram of a two level inverter, we have to take the two steps mentioned above. The calculation of switching sequence and the voltage vector duration times are done by using conventional two level SVPWM methods after simplifications.

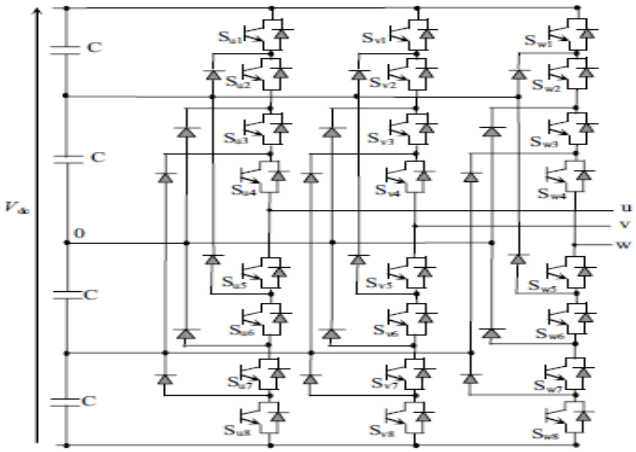

Fig. 5. Three Phase Five-level diode-clamped inverter

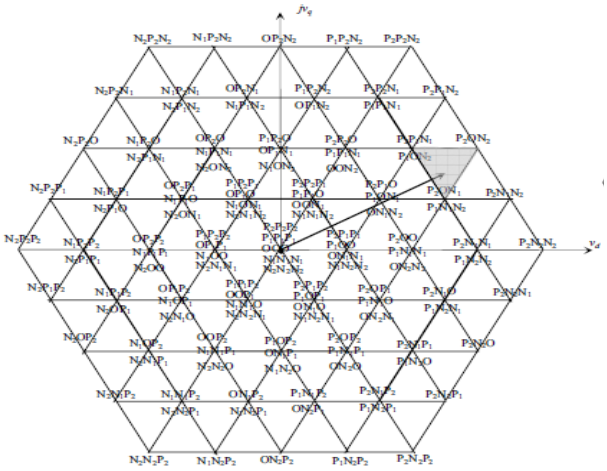

Fig.6. Space vector diagram of Five level inverter

TABLE II. SWITCHING STATE OF FIVE LEVEL INVERTER

Mode	States							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
P_2	1	1	1	1	0	0	0	0
P_1	0	1	1	1	1	0	0	0
O	0	0	1	1	1	1	0	0
N_1	0	0	0	1	1	1	1	0
N_2	0	0	0	0	1	1	1	1

III. CARRIER BASED SPACE VECTOR MODULATION

A novel technique carrier based space vector pulse width modulation (CBSVPM) is described using the concept of effective time. The output voltage is directly calculated by the less times and the voltage modulation technique can be easily simplified in Carrier based SVM The actual gating signals for each inverter arm can be easily deduced as a simple form using the effective time relocation algorithm. CB-SVM allows good and efficient implementation of SVPM without sector determination. The technique is depending on the duty ratio that SVPWM gererates. The higher frequency triangular carrier pulses can be generated on the bases of sinusoidal pulse width modulation and the duty ratio profile. The common mode voltage Injection Method is used to generate CBSVPWM. To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, a common mode voltage, Vcm, is added to the reference phase voltages where the magnitude of Vcm is given by,

$$Vcm = -(Vmax+Vmin)/2 \quad (1)$$

$$Vmax = \max(Van,Vbn,Vcn) \quad (2)$$

$$Vmin = \min(Van,Vbn,Vcn) \quad (3)$$

Where, Vmax = Magnitude of the three sampled maximum reference phase voltages.

Vmin = Magnitude of the three sampled minimum reference phase voltages in a sampling interval.

The addition of the common mode voltage, Vcm results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the SVPWM technique. Eqn (1) is based on the fact that, in an sampling interval, the reference phase which has lowest magnitude (termed the min phase) crosses the triangular carrier first and causes the first transition in the inverter switching state. In a two level SVPWM method, the reference phase, which has the maximum magnitude crosses the carrier last and causes the last switching transition in the inverter switching states.The Simulation model of CB-SVPWM inverter as shown in fig.7. The Output waveforms of CB-SVPWM inverter as shown in fig.8.

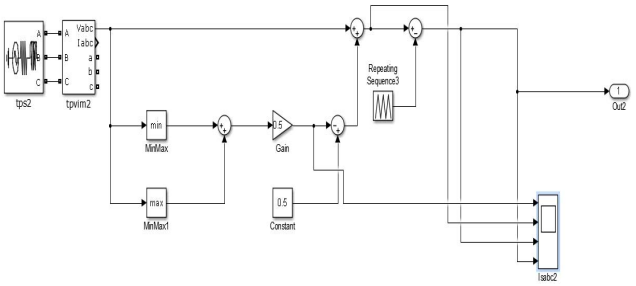

Fig.7. Simulation Model of CB-SVPWM inverter

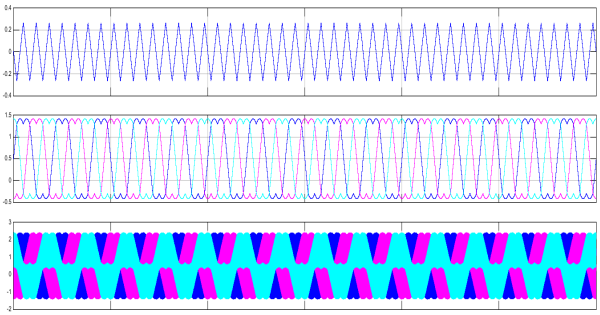

Fig.8. Output waveforms of CB-SVPWM inverter

IV. SIMULATION RESULTS AND ANALYSIS

This simulation was done in the MATLAB software with the DC input voltage.The R-L load is connected to the output terminal of an inverter with the specification given below. Here the same load is considered for all the inverter and the current and voltage waveform are studied with its harmonics analysis. Fig.9.Fig.15 &Fig.21 shows the Simulation diagram of three phase two-level inverter, three level &five level diode clamped inverter respectively. Fig.10.Fig.16 &Fig.22 shows the output line voltage of three phase two-level inverter, three level &five level diode clamped inverter respectively.Fig.11.Fig.17 &Fig.23 shows the output RMS Voltage of three phase two-level inverter, three level &five level diode clamped inverter respectively.Fig.12.Fig.18 &Fig.24 shows the output current of three phase two-level inverter, three level &five level diode clamped inverter respectively.Fig.13.Fig.19 &Fig.25 shows the THD of line voltage of three phase two-level inverter, three level &five level diode clamped inverter respectively. Fig.14.Fig.20 &Fig.26 shows the THD of line current of three phase two-level inverter, three level &five level diode clamped inverter.Table.I shows that switching state and terminal voltage of three level inverter. Table.II shows that switching state of five level inverter. Table.III shows that output voltage & Current THD analysis using CB-SVM.As seen from theFig.16 &Fig.22 the output of five level inverter is more nearer to sine wave than the output of three level inverter. Similarly the output of three level inverter is more nearer to sine wave than the output of two level inverter. And as seen from the Fig.10.Fig.16 and Table III, the total harmonic distortion (THD) reduces as the number of levels increases.

TABLE.III Inverter Ratings

Sr.No	Parameter	Ratings
01	Active power(P)	1000 Watt
02	Reactive power(Q)	750 VAR
03	Total power(S)	1250 VA
04	Power Factor(cosφ)	0.8(lagging)

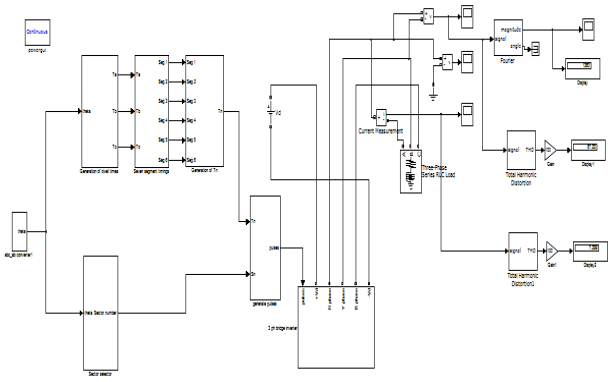

Fig.9. Simulation diagram of three phase two-level inverter

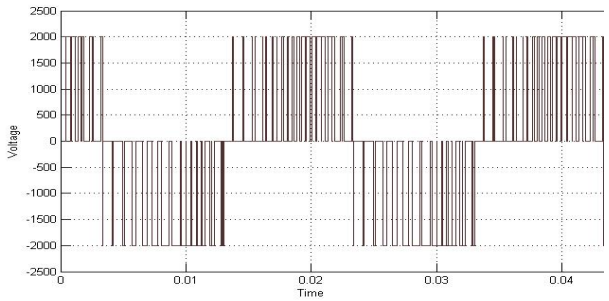

Fig. 10 .Output Line voltage of two-level Inverter

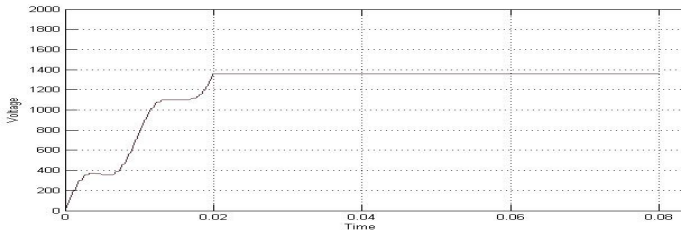

Fig. 11. Output RMS voltage of two-level inverter

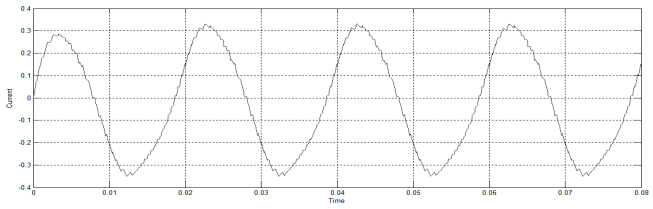

Fig. 12. Output Current waveform of two-level inverter

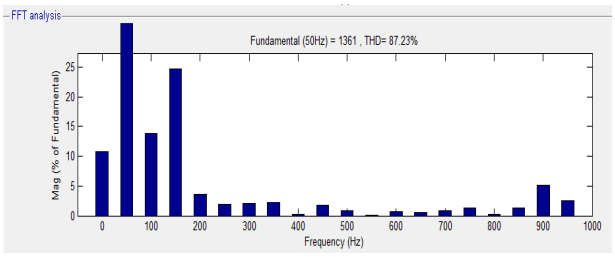

Fig.13..Determination of THD of line voltage of two level inverter

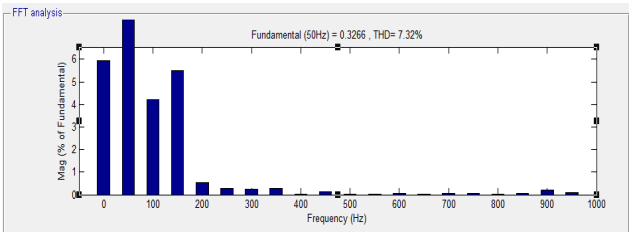

Fig .14.Determination of THD of line current of two level inverter

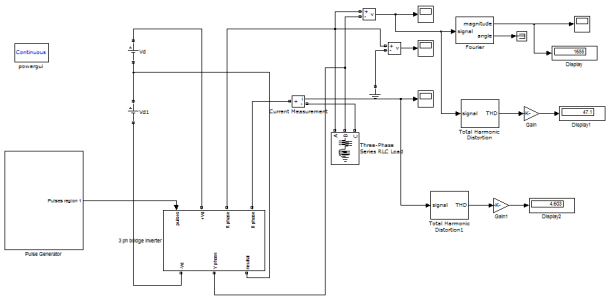

Fig.15. Simulation diagram of Three phase Three-Level Diode clamped Inverter

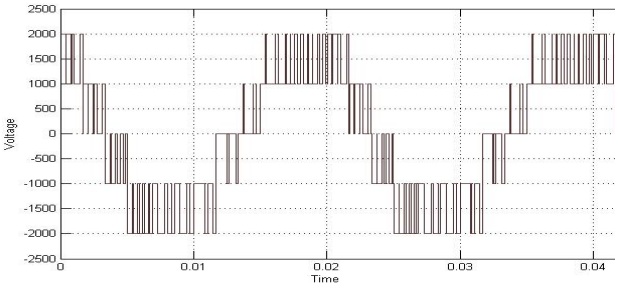

Fig. 16.Output line voltage of three-level Inverter

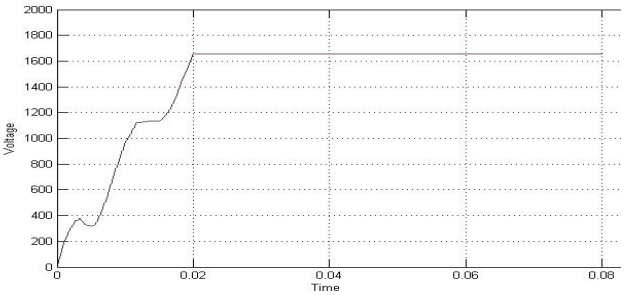

Fig.17. Output RMS Voltage of three-level Inverter

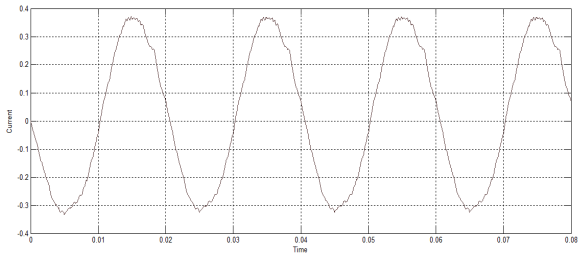

Fig. 18. Output Current waveform of three-level inverter

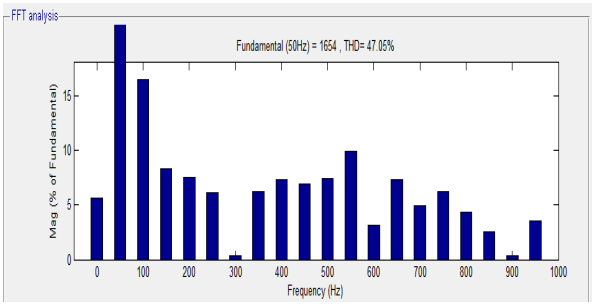

Fig.19.Determination of THD of line voltage of of three-level inverter

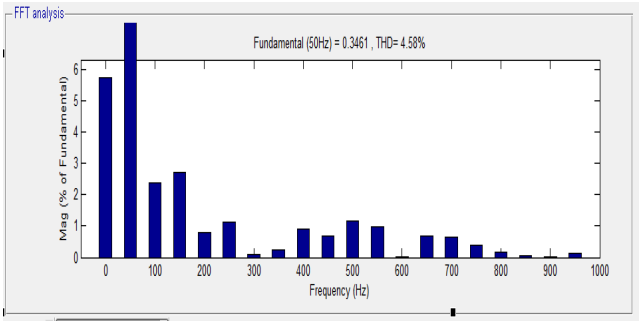

Fig.20.Determination of THD of line Current of three-level inverter

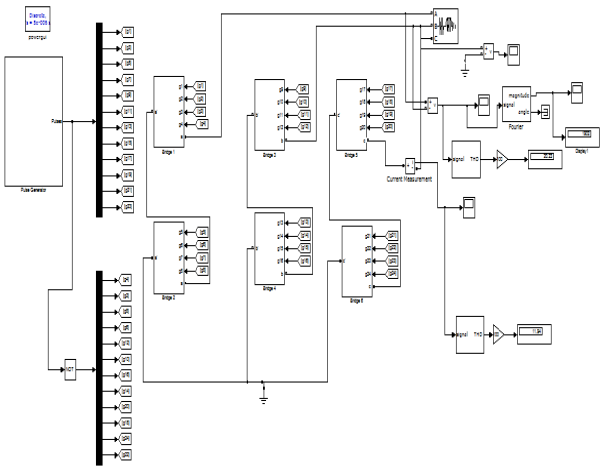

Fig.21. Simulation diagram of three phase five-level diode clamped inverter

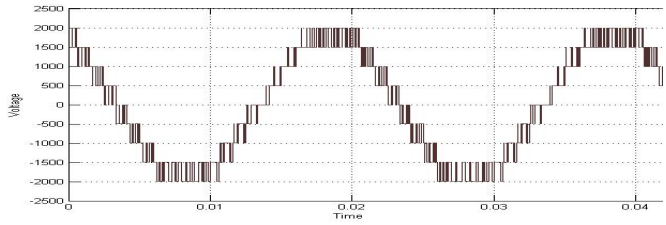

Fig.22. Output line voltage of five-level Inverter

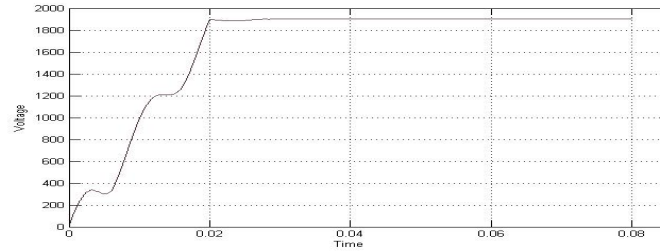

Fig.23. Output RMS Voltage of five-level Inverter

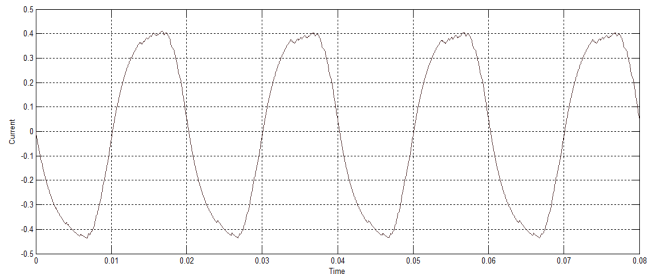

Fig.24. Output Current waveform of five-level inverter

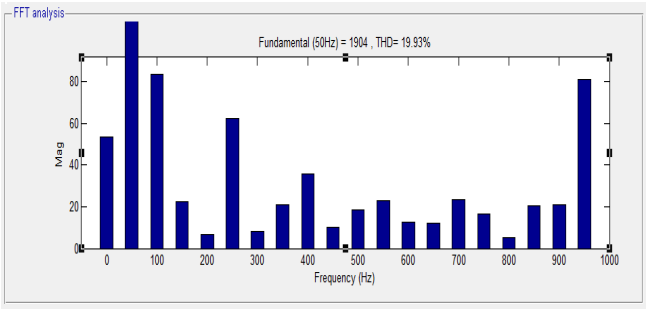

Fig.25.Determination of THD of line voltage of five-level inverter

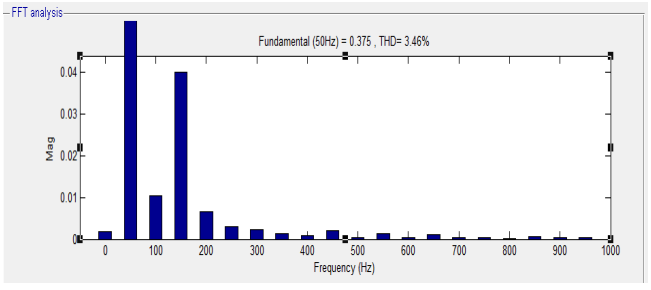

Fig.26.Determination of THD of line current of five-level inverter

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TABLE III. THD ANALYSIS USING CB-SVM

Sr.No	Type of Inverter	Output Voltage in volts	%THD of Voltage	Load Current in Ampere	% THD of Current
01	Two-level VSI	1360	87.22%	0.3266	7.32%
02	Three-level DCMLI	1655	47.09%	0.3467	4.58%
03	Five-level DCMLI	1902	19.93%	0.375	3.46%

V. CONCLUSION

The simulation analysis of three phase VSI, three phase three level diode clamped inverter and five level diode clamped inverter using IGBT's has been done using MATLAB software.The Pulses for the switches have developed using Carrier based Space Vector Modulation technique for two, three & five level diode clamped IGBT's inverters. The output Voltages, currents and THD analysis of two, three&five level diode clamped inverters has been studied. It has been observed from the output voltage waveform that it appears more like sine wave as the number of level increases. This has been in fact proved by doing FFT analysis on the voltage waveforms and it was found that the total harmonic distortion decreases as the number of level increases. This leads to decrease in the requirement of filter. The number of levels of the multilevel inverter to be used for a particular application can thus be decided depending upon the allowed THD.From the results it is concluded that five level inverter can use more dc link voltage than two & three level inverter and also CB-SVM technique utilizes DC bus voltage more efficiently and generates less harmonics.

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